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Model Predictive Current Control with Asymmetric Stacked Multilevel Inverter and LCL-Filter Based STATCOM

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Abstract

The work presented in this paper deals with a proposal of a new topology of a multilevel inverter to act as a Static synchronous Compensator (STATCOM). The proposed inverter is the five-level Asymmetric Stacked Multi-Level Inverter (ASMLI). One of the essential features of this inverter that distinguishes it from the conventional types is that it achieves the required voltage levels with fewer switching devices, leading to simplifying the control process. Moreover, the work includes using a Finite Control Set Model Predictive Current Control (FCS-MPCC) to control the proposed structure. The FCS-MPCC control strategy performs the finite optimization process at the current sampling instant to provide the optimum switching states to the inverter at the next sampling instant. Therefore, this control strategy allows injecting harmonic current and reactive power compensation to reduce source current distortion and improve the voltage profile and power factor. The optimization mechanism reduces the cost function, which is a function of measuring the network current's deviation from the reference value and how the capacitor voltage deviates from the required values. LCL-filter was used to connect this setup to the grid, and its resonance was actively damped using the multivariable capabilities of the FCS-MPCC. The proposed control framework was simulated using MATLAB/Simulink 9.1 environment and tested in a distorted and healthy network compared to a conventional two-level converter with RL-filter. The STATCOM was used to inject reactive power to raise the source power factor to unity and reduce source current harmonics by injecting harmonic current. The proposed prototype could absorb 70% of source current harmonics, which is nearly 25% better than a conventional inverter, inject an appropriate amount of reactive power, and raise the source power factor to unity in two case scenarios. The performance achieved was promising at steady-state operation and speedy response during transients with balanced capacitors voltages.

Keywords: Predictive control; DC-AC power converters; Power conditioning; Current control; Reactive power control; STATCOM

1. Introduction

The increasing loads into the supply systems need significant improvements to the power system utilities used to improve reliability and improve delivered power quality to the customers with the lowest cost possible. In order to achieve these goals, power electronics apparatus are being incorporated into the power system. This technology is known as the flexible AC transmission systems (FACTS) devices family. These devices are static devices connected in series, shunt, or the series shunt to control one or more transmission system parameters that enhance controllability and increase power transfer capability.

The shunt controllers have proven to solve a wide range of transmission and distribution drawbacks [1]. By employing these controllers, the power feeders' transmission capacity could be increased [2]. The voltage profile can be enhanced by injecting a proper amount of reactive power and injecting harmonic current to decrease source harmonics [3]. It can also damp power system oscillation and improve transient stability by high-speed converters used to construct shunt FACTS controllers [4].

Nomenclature			
v	Output voltage vector	L1	Grid side filter inductance
VaN, VbN, VcN	phase voltage of the inverter	L2	Inverter side filter inductance
a	$e^{j2\pi/3.}$	C	Filter capacitance
Vdc	DC-link voltage	Ts	Sampling period
iL	Load current	W_1	the weighting factor for the grid-side current
Vpcc	The voltage of point of common coupling	W_c	the weighting factor for filter capacitors voltage
e	Back EMF	W_2	the weighting factor for inverter side current
LPF	Low pass filter	εc	a penalty imposed on capacitors voltage deviation
I_1, I_1*	Actual and reference grid-side current	W_{fly}	the weighting factor for flying capacitors
I_2, I_2*	Actual and reference inverter side current	W_{DC}	the weighting factor for DC-link capacitors
u_c, u_{c*}	Actual and reference filter capacitor voltage	J	Cost function
I_{ph}	Phase current	wg	Angular frequency of the grid

STATCOM device is one of Shunt FACTS controllers that use a VSI and a passive interfacing element to connect to the grid. VSI can be constructed using 2-level or different multilevel converter topologies [5], [6]. Three voltage levels or more converters are considered multilevel converters; the classical converter uses two levels of six pulse converters limited to few kV levels due to limited semiconductor switch ratings. Therefore, the use of a transformer becomes imposed on employing it on medium voltage levels. Using transformers raises the system cost, size, and weight which can be avoided using a string of switches connected in series. However, this leads to another problem of complicated string design and high cost. In contrast, high voltage levels can be synthesized easily by using multilevel converters. The multilevel converters use a higher number of switches than a two-level converter distributed differently depending on the number of levels and the considered topology; the more number of levels will result in a better quality converter at the expense of increasing complexity, cost, size, and weight. Each switch must have its gating signal, which increases control complexity. Various topologies and control schemes were presented in the literature to solve network problems [7], [8]. Three multilevel topologies are considered conventional topologies: diode clamped multilevel converter, flying capacitor multilevel converter, and cascade H-bridge converter. The conventional five-level topologies are compared in [9]. Each topology suffers from its limitation; the cascade H-bridge requires isolated DC sources that may not be available. The diode clamped converter has an unequal lifetime of switches and difficult voltage balancing of the capacitors with a higher number of levels. The last limitation arises with the flying capacitor converter and limited switching frequency due to the many capacitors used. Different control schemes have been proposed to control the switches' gating, highly dependent upon application, such as PWM and SVM, and recently model predictive control [10]. Another challenge of multilevel converters is voltage balancing of the capacitors due to unequal currents flow that charge/discharge the capacitors and the difficulty in controlling them. Researchers proposed many solutions to design a STATCOM device out of multilevel converters or novel control strategies. [11] Introduces D-STATCOM without capacitor to correct harmonics and power factors. In [12], a 7-level cascade H-bridge with predictive current control operated as STATCOM has been presented, a small error in reference tracks was observed. In [13], a 2-level inverter with a new predictive control approach is used; the conventional two-level inverter puts higher stress on switches than multilevel inverters. [14] Uses predictive control-based space vector modulation to generate pulses for VSI, the use of RL-filter offers less harmonic attenuation than LCL-filter. [15] Uses flying capacitors inverter (FC) with five-level output voltage controlled by level-shifted PWM as STATCOM; in addition to the limitation of FC multilevel inverter mentioned above, the presence of current regulator slows the dynamic response performance.

This paper aims to build a STATCOM prototype to compensate for load harmonics and reactive power needs composing a VSI constructed of a multilevel inverter topology that uses less rating and components than standard two-level inverter and conventional multilevel inverter topologies[16]. The five-level converter is chosen because it can produce a good quality waveform with a reasonable amount of components and control complexity. The proposed five-level ASMLI combines a three-level flying capacitor multilevel inverter with a three-level diode clamped inverter to form a five-level asymmetric topology. This VSI is to be interfaced with the network through a third-order LCL-filter to mitigate harmonics and to reduce inductance and filter losses compared to L-filter; still, it can cause resonance unless it is well damped [17]. Predictive control is an obvious choice for designing such compensators, specifically predictive current control based on the system model. It can handle multiple variables simultaneously and excellent dynamic performance by eliminating the current regulator and modulator, and it can override the inverter and filter challenges [18]. The system's model is constructed to damp the filter resonance and balance the capacitors' voltages without any external circuit. This prototype is simulated using MATLAB/Simulink in a healthy and distorted current network and compared to a two-level conventional converter with an RL filter. Simulation results show that this prototype can solve network problems fastly by injecting reactive power and harmonic current better than the two-level converter. This paper is organized as follows:

Section (1) presents the ASMLI topology and the system modeling with FCS-MPCC. In section (2), simulation results are shown for two network cases with their discussion. Finally, conclusions are drawn in section (3).

2. Proposed Topology and Control Scheme

2.1. Five-level asymmetric stacked multilevel inverter

Figure 1shows one leg of the proposed five-level asymmetric stacked MLI [16]. The topology consists of 8 semiconductor switches, two diodes, two common DC-link capacitors, and two flying capacitors for one leg. It combines three-level FCMLI with three-level DCMLI to form a five-level asymmetric topology with reduced component count and rating. Eight switches work in complementary to each other to reduce control complexity. Voltages of the DC-link capacitors (C11, C12) are maintained at ½ Vdc, while voltages of the flying capacitors (C21, C22) are held at ¼ Vdc. This asymmetric topology has (9) possible switching states from (16) total states that can synthesize five voltage levels. Table 1 summarizes all possible switching states and corresponding voltage levels. Four redundant states are used to balance the voltages of the capacitors at the desired voltage. All switches are rated at ¼ Vdc except S1 and $(S2)^{-}$that are rated at ½ Vdc. This topology has the advantage of a reduced number and rating of components when compared to five-level conventional topologies.

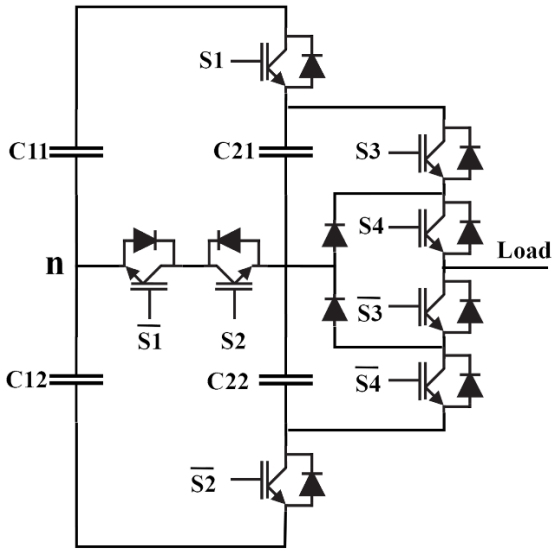


Fig. 1 One leg of ASMLI

Table 1 Possible switching states and their effect on capacitors voltages

Output level	Possible state				Effect on C11		Effect on C12		Effect on C21		Effect on C22	
	S1	S2	S3	S4	IL>0	IL<0	IL>0	IL<0	IL>0	IL<0	IL>0	IL<0
-½ Vdc	0	0	0	0	NE.	NE.	C	D	NE.	NE.	NE.	NE.
-¼ Vdc	0	1	0	0	NE.	NE.	NE.	NE.	NE.	NE.	C	D
	0	0	0	1	NE.	NE.	C	D	NE.	NE.	D	C
0	0	1	0	1	NE.	NE.	NE.	NE.	NE.	NE.	NE.	NE.
	0	0	1	1	NE.	NE.	C	D	D	C	D	C
	1	1	0	0	D	C	N.E.	NE.	C	D	C	D
¼ Vdc	1	1	0	1	D	C	N.E.	NE.	C	D	NE.	NE.
	0	1	1	1	NE.	NE.	NE.	NE.	D	C	NE.	NE.
½ Vdc	1	1	1	1	D	C	NE.	NE.	NE.	NE.	NE.	NE.
NE stands for no effect, C for charging, and D for discharging												

The voltage vectors for each possible switching combination should be calculated to be employed in the FCS-MPCC minimization process. For a three-phase inverter, the voltage vectors are calculated as follows

$$v = \frac{2}{3}(v_{aN} + \mathbf{a}v_{bN} + \mathbf{a}^2 v_{cN}) \quad (1)$$

$$v_{xN} = \frac{V_{DC}}{4}(S_{1x} + S_{2x} + S_{3x} + S_{4x})\Big|_{x=a,b,c} \quad (2)$$

2.2. LCL-Filter

VSI is commonly connected to the grid network by first-order L-filter or third-order LCL-filter. The latter offers more harmonic attenuation with less inductance needed, reducing system weight, size, and price compared to L-filters [19]. However, it can cause grid resonance because of capacitive and inductive components used unless it is damped. The damping process can be made passively by introducing resistance in series with a filter capacitor which raises losses and size, or can actively damp by utilizing FCS-MPCC multivariable handling capability. The latter is used in this paper by making the benefit of filter capacitor voltage, inverter side current, and grid side current to damp filter resonance effectively without additional elements required.

2.3. Finite control set model predictive current control (FCS-MPCC)

Advances in digital microprocessors make it possible to control fast processes such as VSI by model predictive control (MPC). It uses the discrete nature of VSI with a limited number of switching states to predict controlled variables' future behavior. MPC control strategy [20] is shown in Figure 2. The load can be a three-phase motor, grid network, or any electrical load. The control process's primary goal is to make the controlled variable (x) follow its desired reference (x*). The controlled variable can be speed, torque, voltage, current, and the variable is measured at the sample (k), and then its future behavior is predicted for each possible switching combination. After that, a minimization process to select the best switching combination makes the variable (x) follow its desired reference [20].

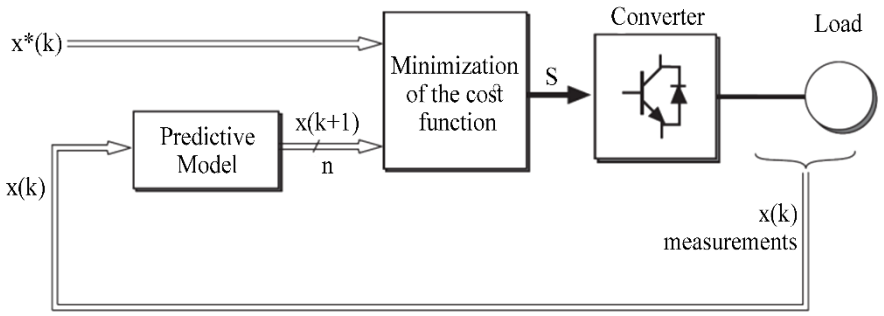


Fig. 2 MPC control strategy

For the proposed topology, a three-phase ASMLI is connected to the grid through LCL-filter [21], as shown in Figure 3. The prediction process begins by reading network information in the stationary reference frame (alpha-beta). The information needed is inverter side current (i2), grid side current (i1), filter capacitors voltage (Uc), and grid voltage at the point of the common coupling (PCC).

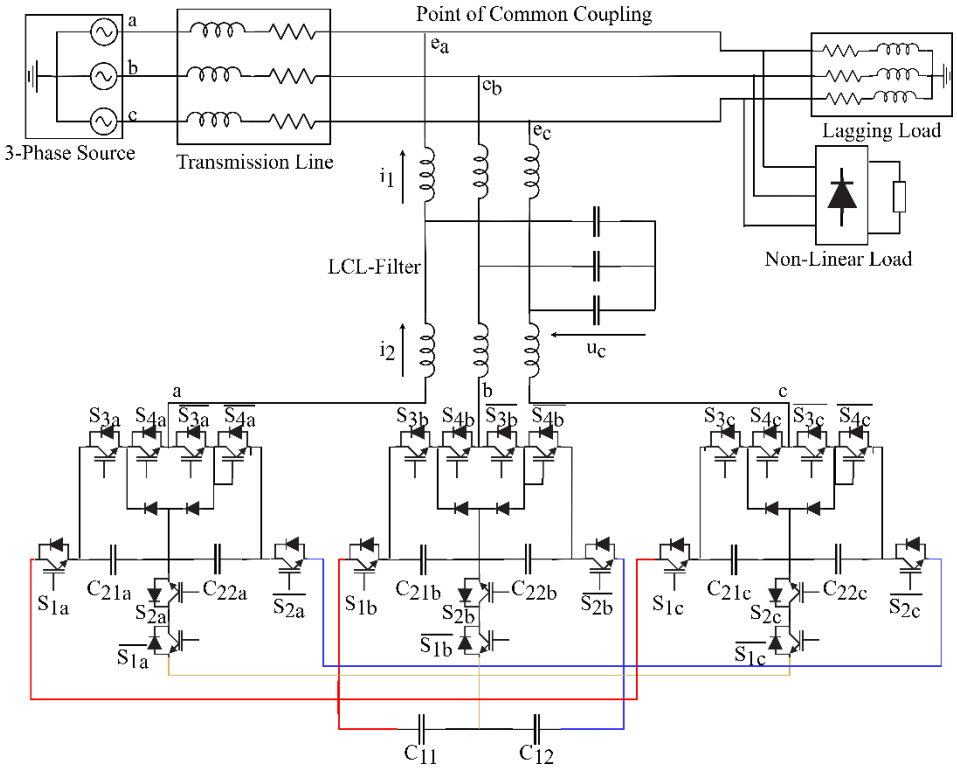


Fig. 3 System configuration

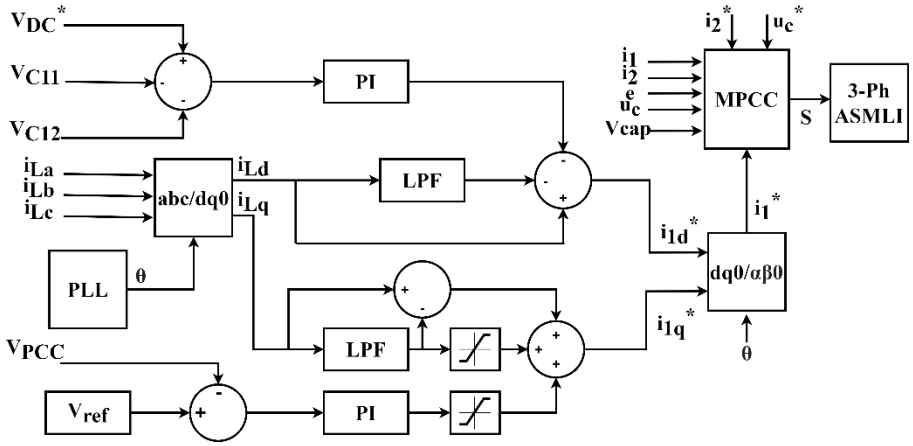


Fig. 4 STATCOM control block diagram

For the STATCOM application, the determination of the grid reference current (i1*) results from the load current in the synchronous reference frame (dq0) [11], [22], as shown in Figure 4. The STATCOM will supply harmonic current of the load plus reactive current limited to the STATCOM rating to improve voltage profile and power factor. The future reference current is achieved using extrapolation to compensate for delay time in reference tracking of sinusoidal reference using the formula:

$$\hat{i}_1^*(k+1) = 3i_1^*(k) - 3i_1^*(k-1) + i_1^*(k-2) \quad (3)$$

Equation 3 determines the reference current's one-step prediction, repeating the above formula to achieve the two-step prediction as shown in equation 4.

$$\hat{i}_1^*(k+2) = 3i_1^*(k+1) - 3i_1^*(k) + i_1^*(k-1) \quad (4)$$

In the same manner, the one-step and two-step future values of the grid voltages are as follows;

$$e(k+1) = 3e(k) - 3e^*(k-1) + e(k-2) \quad (5)$$

$$e(k+2) = 3e(k+1) - 3e(k) + e(k-1) \quad (6)$$

The reference current for filter capacitors voltages and inverter side current calculated as follows [23]–[26]:

$$u_c^* = e - jw_g L_1 i_1^* \quad (7)$$

$$i_2^* = i_1^* - jw_g C u_c^* \quad (8)$$

The predicted future system currents and voltage for all possible switching states can be determined as follows:

$$\Delta i_2(k+1) = \frac{u_c(k) - jw_g L_2 i_2(k) - v(k+1)}{L_2} T_s \quad (9)$$

$$i_2(k+1) = i_2(k) + \Delta i_2(k+1) \quad (10)$$

$$\Delta u_c(k+1) = \frac{i_1(k) - jw_g C u_c(k) - i_2 - 0.5\Delta i_2(k+1)}{C} T_s \quad (11)$$

$$u_c(k+1) = u_c(k) + \Delta u_c(k+1) \quad (12)$$

$$\Delta i_1(k+1) = \frac{e(k) - jw_g L_1 i_1(k) - u_c(k) - 0.5\Delta u_c(k+1)}{L_1} T_s \quad (13)$$

$$i_1(k+1) = i_1(k) + \Delta i_1(k+1) \quad (14)$$

The second step (k+2) was repeating the above calculations by shifting forward one sample. Considering the same voltage vector for delay compensation and reducing computational burden [27], as shown in Figure 5. For a sinusoidal reference, it is preferable to use the two steps or higher prediction over one-step prediction [20].

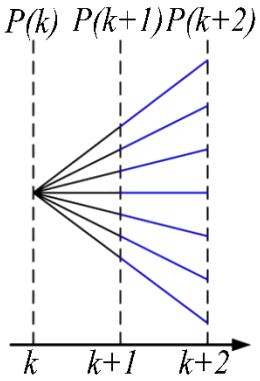


Fig. 5 Two-step prediction MPC

Maintaining voltages of all VSI capacitors at the desired reference; otherwise, it may cause the capacitors to be damaged by overvoltage unless it is oversized or can produce additional undesired THD due to unbalanced voltages. The multivariable handling capability of FCS-MPCC can be functioned to include the capacitors' voltages into the cost function, hence imposing a penalty on the switching combination that causes capacitors voltages to drift from their desired reference. The voltages of the capacitors are predicted for each switching combination by:

$$V_{Cxx}(k+1) = V_{Cxx}(k) + \frac{1}{Cxx} i_{Cxx} T_s \tag{15}$$

The subscript xx refers to the number of the capacitor.

For the ASMLI topology used, the capacitors current equations are extracted from table (1) for one leg, and these currents are determined as follows:

$$i_{C11} = S_1 S_2 i_{ph} \tag{16}$$

$$i_{C12} = (1 - S_2) i_{ph} \tag{17}$$

$$i_{C21} = (S_1 - S_3) i_{ph} \tag{18}$$

$$i_{C22} = (S_2 - S_4) i_{ph} \tag{19}$$

Where S_x is the switch state for each switching combination

$$\begin{aligned} \varepsilon_c = W_{fly} \Bigg(& \left(\frac{V_{ref}}{4} - V_{C21a}(k+1)\right)^2 + \left(\frac{V_{ref}}{4} - V_{C22a}(k+1)\right)^2 + \left(\frac{V_{ref}}{4} - V_{C21b}(k+1)\right)^2 + \left(\frac{V_{ref}}{4} - V_{C22b}(k+1)\right)^2 \\ & + \left(\frac{V_{ref}}{4} - V_{C21c}(k+1)\right)^2 + \left(\frac{V_{ref}}{4} - V_{C22c}(k+1)\right)^2 \Bigg) \\ & + W_{dc} \left(\left(\frac{V_{ref}}{2} - V_{C11}(k+1)\right)^2 + \left(\frac{V_{ref}}{2} - V_{C12}(k+1)\right)^2 \right) \end{aligned} \tag{20}$$

Finally, the cost function to select the best switching combination that makes the STATCOM supplied current follows the calculated reference as follows:

$$\begin{aligned} J = W_1 ((i^*_{1\alpha}(k+1) - i_{1\alpha}(k+1))^2 + \left(i^*_{1\beta}(k+1) - i_{1\beta}(k+1)\right)^2) + W_c ((u^*_{c\alpha}(k+1) - u_{c\alpha}(k+1))^2 \\ + \left(u^*_{c\beta}(k+1) - u_{c\beta}(k+1)\right)^2) + W_2 ((i^*_{2\alpha}(k+1) - i_{2\alpha}(k+1))^2 + \left(i^*_{2\beta}(k+1) - i_{2\beta}(k+1)\right)^2) + \varepsilon_c \end{aligned} \tag{21}$$

The subscripts α and β represent the preceding variable's alpha and beta components on the stationary reference frame.

3. Results and discussion

A MATLAB/Simulink software package offers the tools to implement the proposed prototype; the model is constructed as shown in Figure 6. Figure 7 Achieving the testing process according to two simulation cases, table 2 shows the simulation parameters.

Table 2 Simulation parameters

Parameter	Value
System frequency	50 Hz
Smapling time / Switching frequency	25 µSec / 40 KHz
DC-link voltage setpoint	3000 V
DC-link capacitors	5000 µF
Flying capacitors	2500 µF
Filter capacitor	2 µF
Filter inverter side inductor	5 mH
Filter grid side inductor	2 mH

Case (1): Connecting the STATCOM prototype with one-step prediction to a harmonically distorted network with a lagging load, as shown in Figure 3. The aim is to test the harmonic and reactive current compensation capabilities of the proposed system configuration. The load current possesses a high distortion because of the presence of the nonlinear load. A step-change in load occurs at a time (0.2 Sec), and before connecting the STATCOM, the source must supply the load current shown in Figure 8.

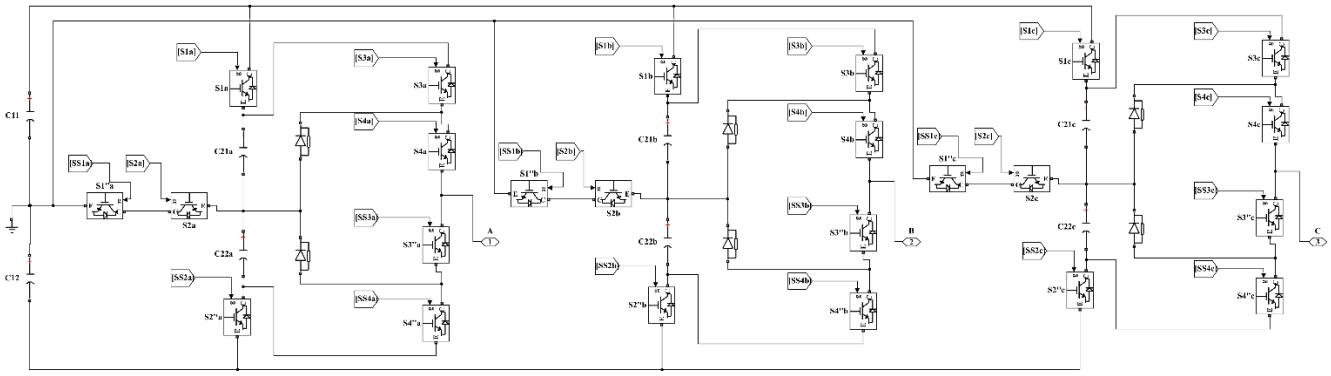


Fig. 6 ASMLI configuration in MATLAB / Simulink

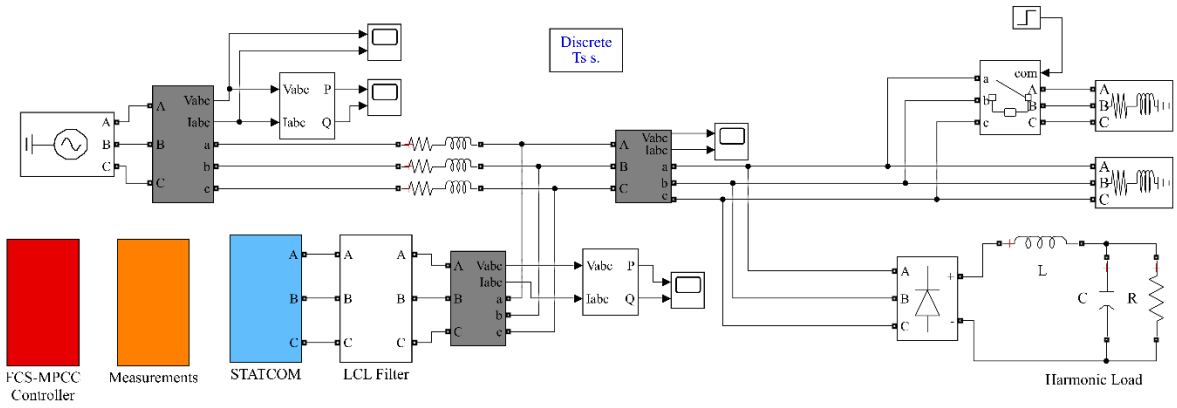
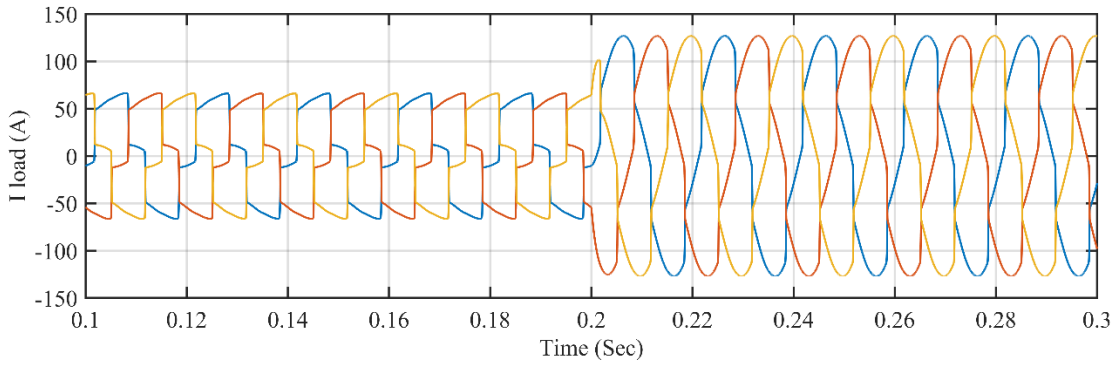
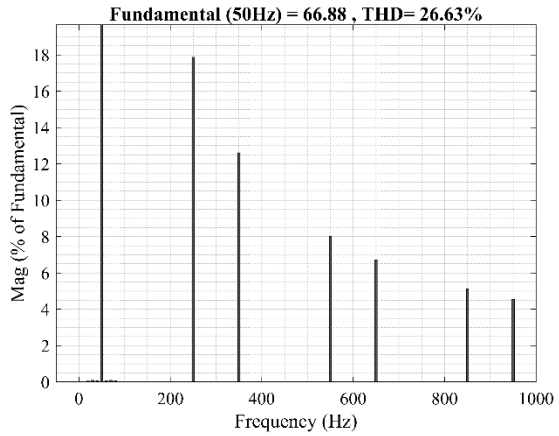


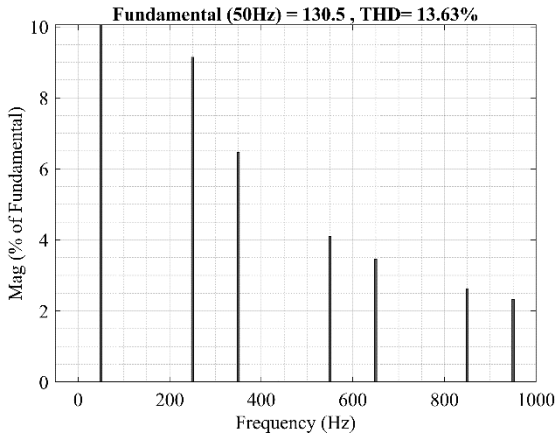
Fig. 7 MATLAB / Simulink model



(a)



(b)



(c)

Fig. 8 (a) Load current, (b) FFT analysis for load current (0.1-0.2 Sec), (c) FFT analysis for load current (0.2-0.3 Sec)

Adding the STATCOM to the network could absorb nearly 70% of harmonics in the source current. It reduced its THD from 26.63% to 7.62% and from 13.6% to 4.32%, as shown in FFT analysis, also supplied all reactive power that the load demands and fastly raised the source power factor to unity in one electrical cycle. Figure 9 shows the source current with STATCOM installed in the network with FFT analysis for both load cases.

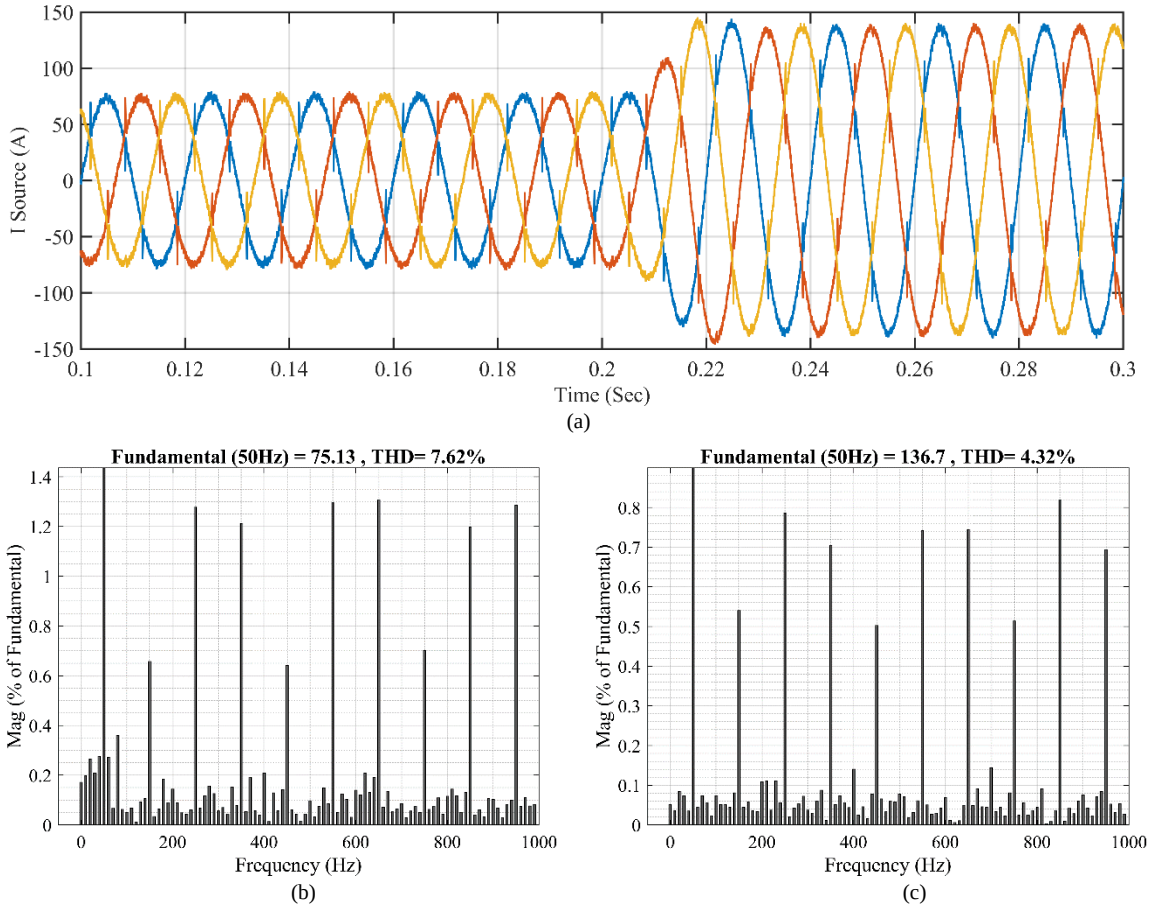


Fig. 9 System configuration with the proposed STATCOM (a) Source current, (b) FFT analysis for source current (0.1-0.2 Sec), (c) FFT analysis for source current (0.2-0.3 Sec)

For the previously mentioned step change in the load that occurred at the time (0.2 Sec), the STATCOM shows an excellent current reference tracking, observing no overshoot or errors in tracking during the event. The actual current follows its desired reference perfectly as the change predicted. Figure 10 shows the reference and actual currents in the stationary reference frame at the moments of load are changed.

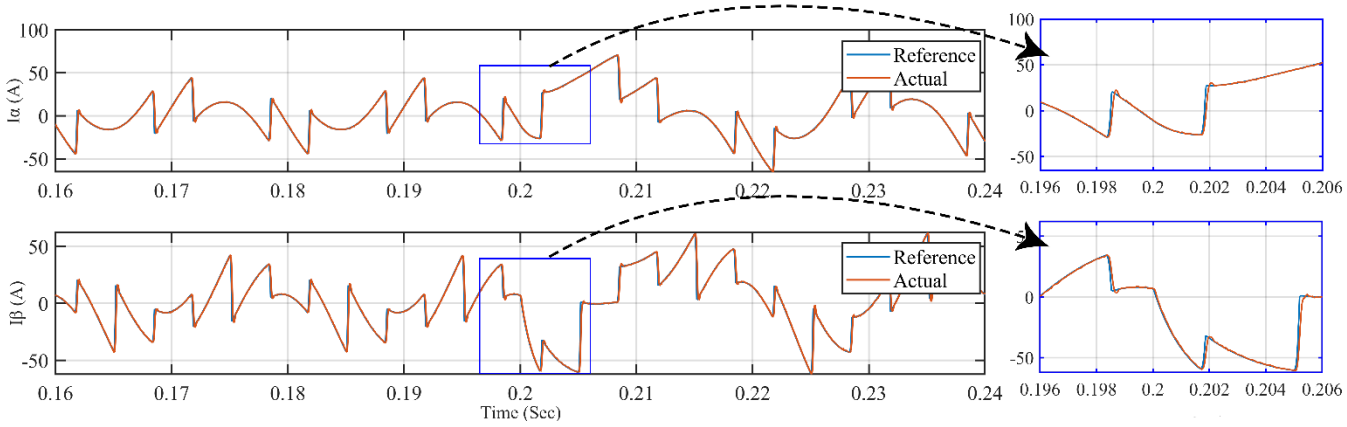


Fig. 10 Current reference tracking in the stationary reference frame for the proposed prototype

It is helpful to compare the proposed topology's performance with another STATCOM design at the same switching frequency and load. Figure11 shows the source current with six pulses, a two-level converter, and an RL filter. Figure 12 shows the reference tracking in a stationary reference frame for a two-level converter, and **Error! Reference source not found.** demonstrates the difference in source current THD for the proposed and conventional models.

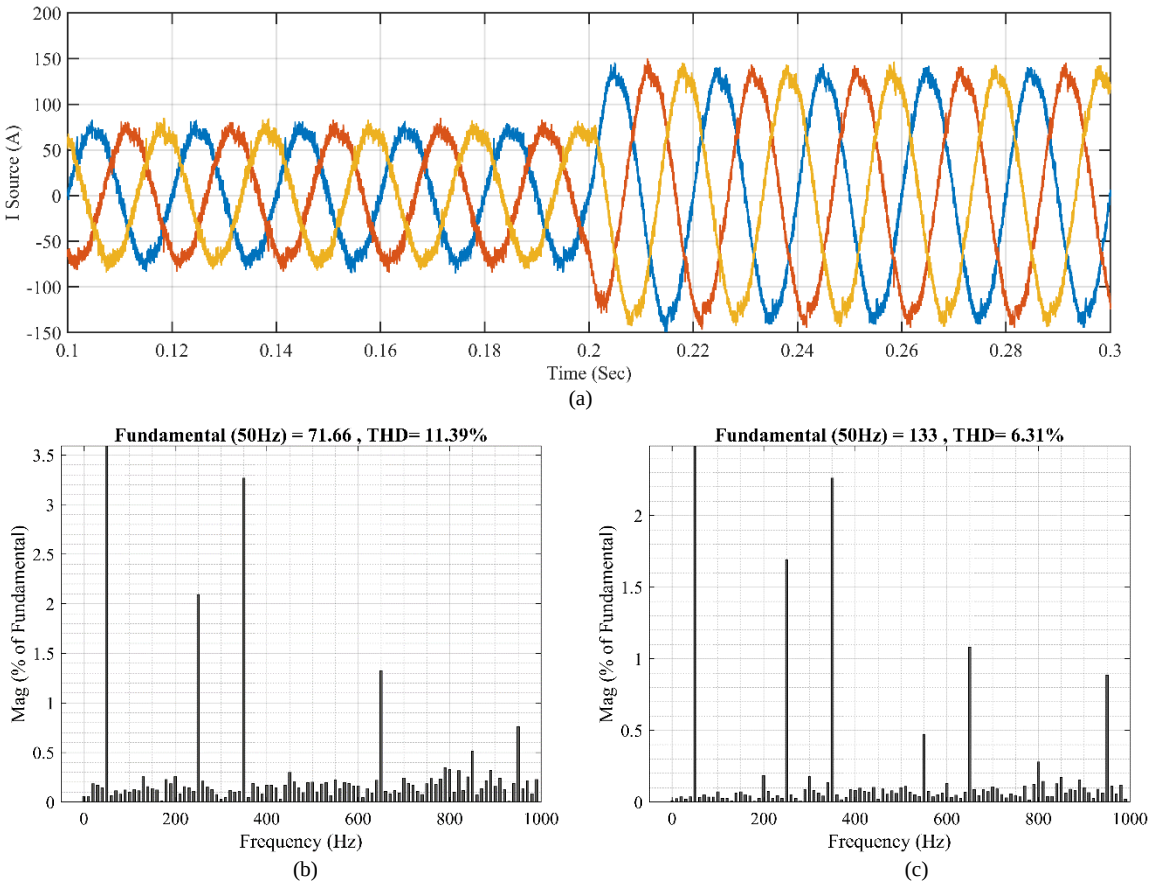


Fig. 11 System configuration with two-level converter STATCOM (a) Source current, (b) FFT analysis for source current (0.1-0.2 Sec), (c) FFT analysis for source current (0.2-0.3 Sec)

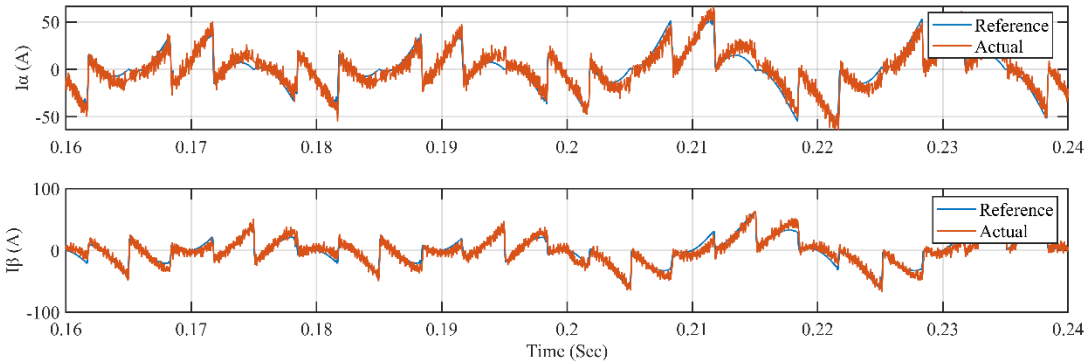


Fig. 12 Current reference tracking in stationary reference frame for two-level converter

Table 3 proposed prototype performance comparison with a conventional converter in terms of source current harmonics mitigation

Model	Current	THD		Overall performance
		0.1-0.2 Sec	0.2-0.3 Sec	
Conventional	Source	11.39 %	6.31 %	≈ -25 % Worse
	Load	26.63 %	13.63 %	
	Improvement	57.22 %	53.7 %	
Proposed	Source	7.62 %	4.32 %	≈ +25 % Better
	Load	26.63 %	13.63 %	
	Improvement	71.38%	68.3 %	

Case (2): Connecting the prototype of the STATCOM with two-step prediction to a healthy network for reactive power compensation to test the proposed configuration with normal balanced loads. As a result, the STATCOM supply current with excellent quality (a THD of less than 1.5%). Similar to case (1), change in the load occurs at (0.2 Sec); the dynamic response is excellent, fast with no errors, as shown in Figure 13. Comparing the proposed prototype with the same six-pulse two-level converter, the latter produces injected current with a higher harmonics distortion and slower dynamic response with up to 3 cycles to adjust to the new state.

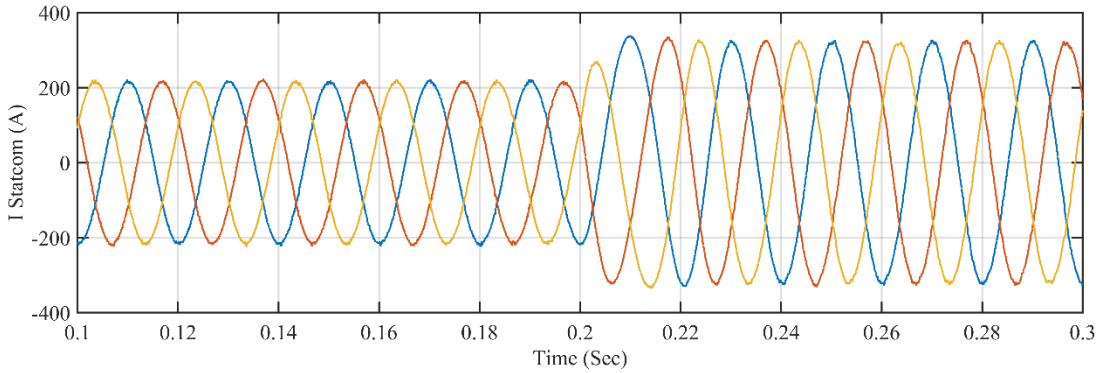


Fig. 13 The step-change in STATCOM current on a healthy network

Figure 14 shows similar responses for both cases (1 and 2) of the DC-link capacitors' voltages during a step change in load. Figure 15 indicates the reactive power compensation and power factor for the three phases at the instant of adding STATCOM (0.2 Sec) to the network. Figure 16 shows reference current tracking in the stationary reference frame when adding the STATCOM to the network at the time (0.2 Sec).

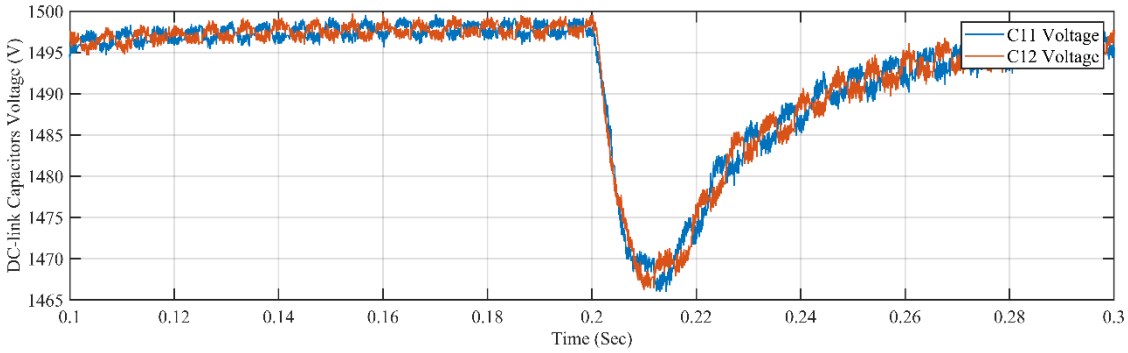
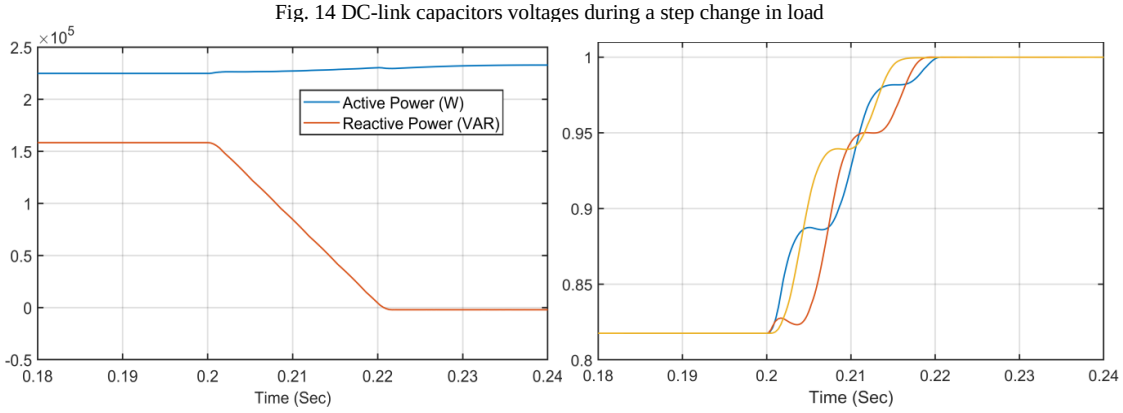


Fig. 14 DC-link capacitors voltages during a step change in load



(a) (b)

Fig. 15 (a) Source active and reactive power, (b) Source power factor

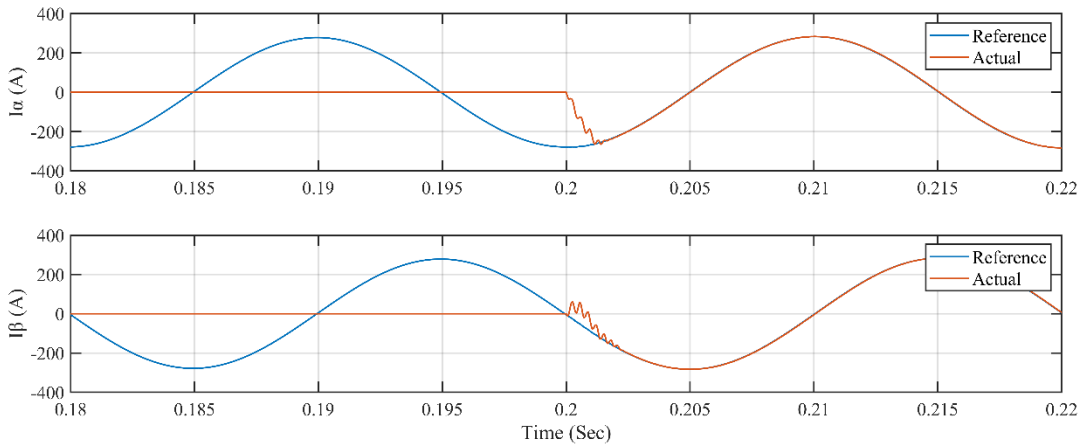


Fig. 16 Current reference tracking the moment of adding STATCOM to the network

Simulation results show an excellent performance of the suggested setup. The STATCOM improved the source current's quality, brought it to the permissible limits, and injected a perfect quality current to improve the power factor. Also, the dynamic performance during the addition of STATCOM to the network and a step-change in load was fast and accurate with balanced capacitors voltages. It was, moreover, achieving the reference tracking almost instantaneously. The comparison between the proposed prototype with a two-level converter with RL filter shows a clear advantage in injected current quality and speed and the reduced rating components needed to construct the STATCOM.

4. Conclusion

This paper presents a new prototype of STATCOM for power factor correction and harmonic current mitigation. The proposed combination of five-level ASMLI topology with model predictive current control and LCL-filter for harmonic and reactive power compensation is a promising candidate to be used in medium voltage networks. The less component number and rating of ASMLI is an advantage over two-level converter and similar five-level topologies. The prediction capabilities of FCS-MPCC were able to solve LCL-filter resonance problems and the capacitor's unbalanced voltage problem besides eliminating linear current regulator (PI) and modulators. The resulting configuration is found to be robust and effective. It neutralized 70% of source current harmonics, nearly 25% better than the conventional two-level converter. It injected reactive power to the grid, which raised the source power factor to unity in one electrical cycle besides speedy transient response during a step change in load far better than conventional two-level converter as proven in simulation results which makes it a preferable choice than conventional converter. One improvement that can be made in the future is to reduce the computations on the controller to make it possible to be implemented practically in low-cost pieces of equipment.

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