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A VHDL Code for Offset Pulse Position Modulation Working with Reed Solomon System by Using ModelSim

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Abstract

Error correction codes, often known as ECC, play a significant part in the process of detecting and correcting data mistakes that occur through communication channels that are unreliable or noisy. The essential concept behind error correction through ECC is to supplement the message that is being sent by the transmitter with redundant bits, the values of which are determined by the parameters n and k. These bits can then be utilized by the receiver to identify and correct specific types of errors. ECC is utilized in a wide variety of applications, including but not limited to data storage, the Internet, and telecommunications. There are numerous variations of ECC, including linear block, convolutional, and turbo codes, among others. The results of a simulation of a linear block reed Solomon, for example, with offset pulse position modulation have been presented in this study. The simulation was carried out in very high-speed integrated circuit hardware description language (VHDL), and a field-programmable gate array was used (FPGA) It made use of a Boolean function to function to program code for an algorithm that is working. Because of its performance, time to market, cost, reliability, and long-term maintenance benefits, FPGA is an appropriate platform for implementing error correction code (ECC). As a part of this project, the technique of offset Pulse Position Modulation (Offset PPM) was invented as an outstanding solution to code the fiber-optic applications and Reed Solomon (RS) codes apply to ModelSim SE-64 10.5 software. In addition, this coding scheme has been approved by the simulation and is matched with theory, and it is expected to be implemented shortly. The study begins with a concise introduction to RS encode/decode about design and performance and then moves on to discuss the development result of simulation and hardware implementation.

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Keywords: VHDL; ECC; FPGA; RS; OPPM; ModelSim

1. Introduction

Due primarily to its low mark-to-space ratio, digital pulse position modulation (D-PPM) provides an exceptionally high level of sensitivity when it comes to the encoding of huge data words. Sibley has lately suggested the implementation of a brand-new coding method known as offset PPM. The line rate will become half of what it would be at the comparable digital PPM when using offset PPM, which employs the notion of a sign bit. The ease of use of this coding method is another benefit to utilizing it. In addition to it, the sensitivity is increased by three decibels compared to digital PPM [1]. In most cases, we require that the modulation be one that can be reversed so that the message may be reconstructed with the proper demodulation procedure. The goal of utilizing error correction codes can be summed up as increasing the reliability of data communication over a noisy channel as well as controlling errors to obtain reliable reproduction (Recovery) of data [2]. These are just two of the many possible ways in which this goal can be expressed. Reed-Solomon error-correcting codes, also known as RS codes, are extensively utilized in data storage and communication systems to recover data from possible errors that occur during the process of data transfer. These are also very robust in symbol errors correction as well as burst errors. The benefits and uses of FPGA have led to the development of a new and more advanced field of study known as reconfigurable technology [3]. The flexible hardware can be reconfigured by factors that govern the logic design scheme based on the algorithms' similarities. This allows the hardware to be used in a variety of diverse applications. As a result, a reprogrammable RS Decoder might be developed to cut down on the amount of hardware required and the level of complexity [4]. Reed-Solomon encoders and decoders have been developed in this research by executing VHDL models of various units of encoder and decoder and collecting synthesis reports. In addition, ModelSim SE-64 10.5 software has been utilized to acquire simulation waveforms.

1.1. VHDL Code

VHDL is an acronym for Very high-speed hardware language. It is software that models digital systems using structural modeling methods, behavioural and dataflow, and it is used to represent these systems. This language was initially presented to the public for the very first time by the Department of Defense (DoD) in the year 1981 as part of the Very High-Speed Integrated Circuit (VHSIC) program [5].

Nomenclature & Symbols			
LSB	Least significant bit	OPPM	Offset Pulse Position Modulation
PCM	Pulse code modulation	MPPM	Multi-Pulse pulse position modulation
VLC	Visible Light Communication	PRBS	Pseudo-random binary sequence
DoD	Department of defence	s	mistakes
RS-EC	Reed–Solomon Erasure Code	r	erasures
LSB	Least significant bit	n	Length of the codeword
RS	Reed Solomon	k	Length of the source data
ECC	ERROR correction code	VHDL	Very high-speed integrated circuit hardware description language
FPGA	Field-programmable gate array	D-PPM	Digital pulse position modulation

Numerous studies have been conducted on FPGAs with RS, one example being " Reed-Solomon Algorithm for FPGA Area Optimization in Space Applications." An algebraic approach to the design of RS algorithms is demonstrated in this research, and it leads to a final FPGA implementation that uses less space than standard implementations do. The algebraic approach to RS algorithm design yielded this result. [5] Decoding Decoders for the Reed–Solomon Erasure Code (RS-EC) with Fault Detection and Location in User Memory" To begin with, theoretical analysis and fault injection experiments are used to demonstrate that the FPGA implementation of the RS-EC decoder is highly resistant to SEUs [6]. " Reed Solomon Encoder/Decoder Implementation Using Spartan FPGA." After that, a top-level schematic design is needed to describe the pins that are necessary for the actual hardware interface. A programming file is eventually downloaded to the FPGA board once the compilation has been completed successfully, timing analysis has been obtained, and synthesis reports have been generated. The functionality of the VHDL code is seen in Fig. 1.

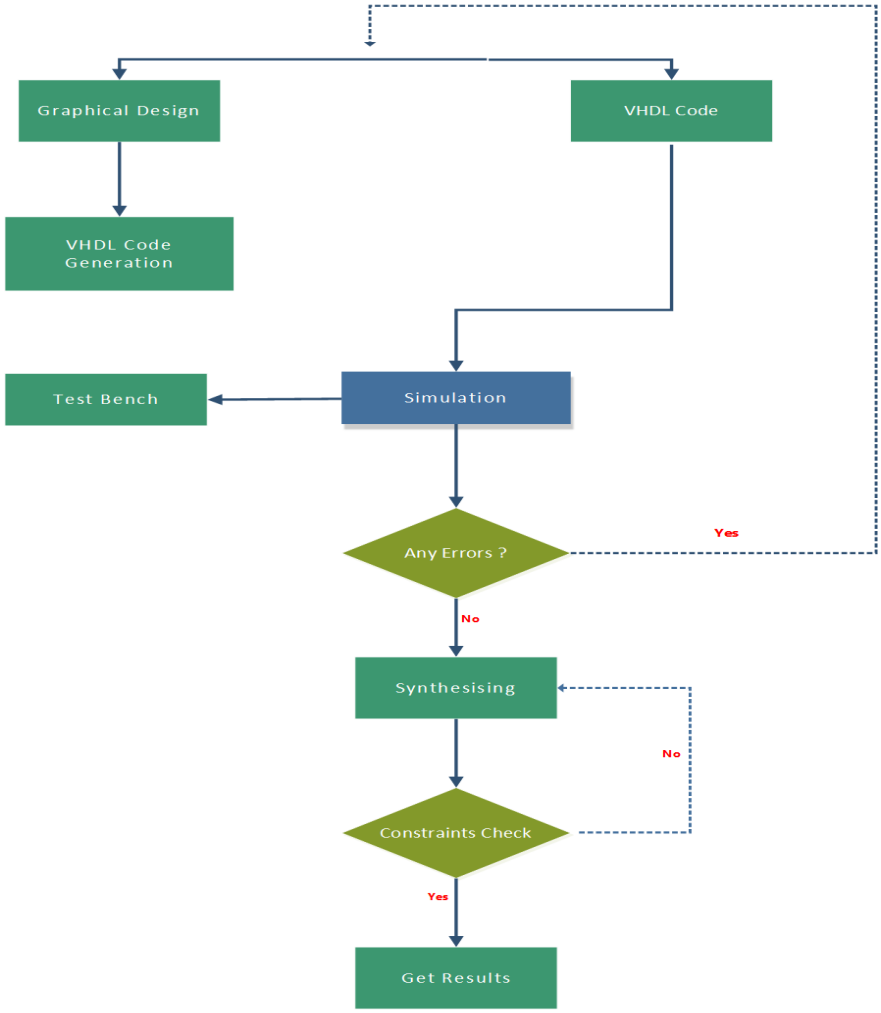

Fig. 1. VHDL Implementation flow chart

1.2. Reed Solomon Theory

The Reed Solomon (RS) codes belong to the same category as other linear block codes and are a subset of the BCH code set. To specify an RS code using s-bit symbols, the format RS (n, k) must be used. This indicates that the encoder creates an n-symbol codeword by taking k data symbols, each of which consists of s bits, and adding parity notation. There are n minus k parties, and every one consists of s bits. The number

of symbols in a codeword that an RS decoder can fix is limited to t, with 2t being equal to n minus k. A decoder can erase up to two times as much data as it can correct [7]. When it comes to the decoder, three different scenarios could result in a codeword being decoded.

1- The original codeword that was transmitted can always be recovered if the condition (2s+r2t) (s mistakes, r erasures) is met.
2- The decoder discovers that it is unable to retrieve the codeword that was first input and shows this information.
3- Incorrect decoding and retrieval of the codeword by the decoder, and there is no indication that this has occurred.

If the length of the codeword is n and the length of the source data is k, the error correction capability can be described as t = (n-k)/2 in RS (n, k). The chance of each of these three options depends on the precise RS code that was selected, the number of errors, and the distribution of the errors. To summarize, a standard RS codeword typically contains k symbols for the source data and n-k symbols for redundancy (parity check) [8]. RS encoders can be constructed by LFSRs, while RS decoders are more difficult to design. Figure (2). The output of the encoder and decoder, Reed Solomon, was achieved by the application of ModelSim.

1.3. Offset Pulse position modulation (OPPM)

Offset Pulse Position Modulation, noted as OPPM for short, was utilized as a novel form of digital pulse position modulation, or DPPM for short. This kind of modulation may be preferred for use in optical and free-space communication. The OPPM functions at a speed that is only half that of the allowed rates for the digital PPM, but it improves the low bandwidth sensitivity [9]. Meaning, OPPM is given to solve the problems associated with the extension of the bandwidth of pulse position modulation (PPM). It is interesting to note that the OPPM improves the sensitivity by more than 3.1 dB in comparison to digital PPM, and its sensitivity is adequate in comparison to that of multiple PPM. The process of error correction might be located anywhere within a group of sequences to be studied. When all of the codeword positions have been brought back to zero, the initial sequence has been applied. The least significant bit (LSB) is the bit that is thrown away in the second sequence so that the first sequence can be used instead. The following code words will be added for being formed whenever a digit is moved from the least significant position to the most significant position to produce them. Researchers from Ahfayd et al. investigated the spectrum properties of truncated PPM, MPPM, and OPPM. As a result of this, it has been determined that the OPPM is capable of producing different lines in comparison to the DPPM [10]. On the other hand, when compared to OPPM, DPPM possesses a robust element frame of repetition rate. In pulse code modulation (PCM), three-bit codewords can be converted to four-bit codewords through the use of the OPPM technique. On the other hand, DPPM has a line rate of 2m, and within the fundamental PCM rate, the m percent of the m-bits are considered to be signal bits. Additionally, the letter m can be used to demonstrate how to convert three bits of PCM into OPPM and DPPM codewords Table 1. For example, the approach is analogous to DPPM when applied at a concentration of 100 PCM. On the other hand, there will not be a pulse broadcast for 000 PCM when the OPPM is differential. The PCM term is removed from the MSB, and it is delayed by 2 m-1 time slots when it is passed via the decoder and OPPM coder [11]. Fig. 2 displays the Offset PPM VHDL code sequence.

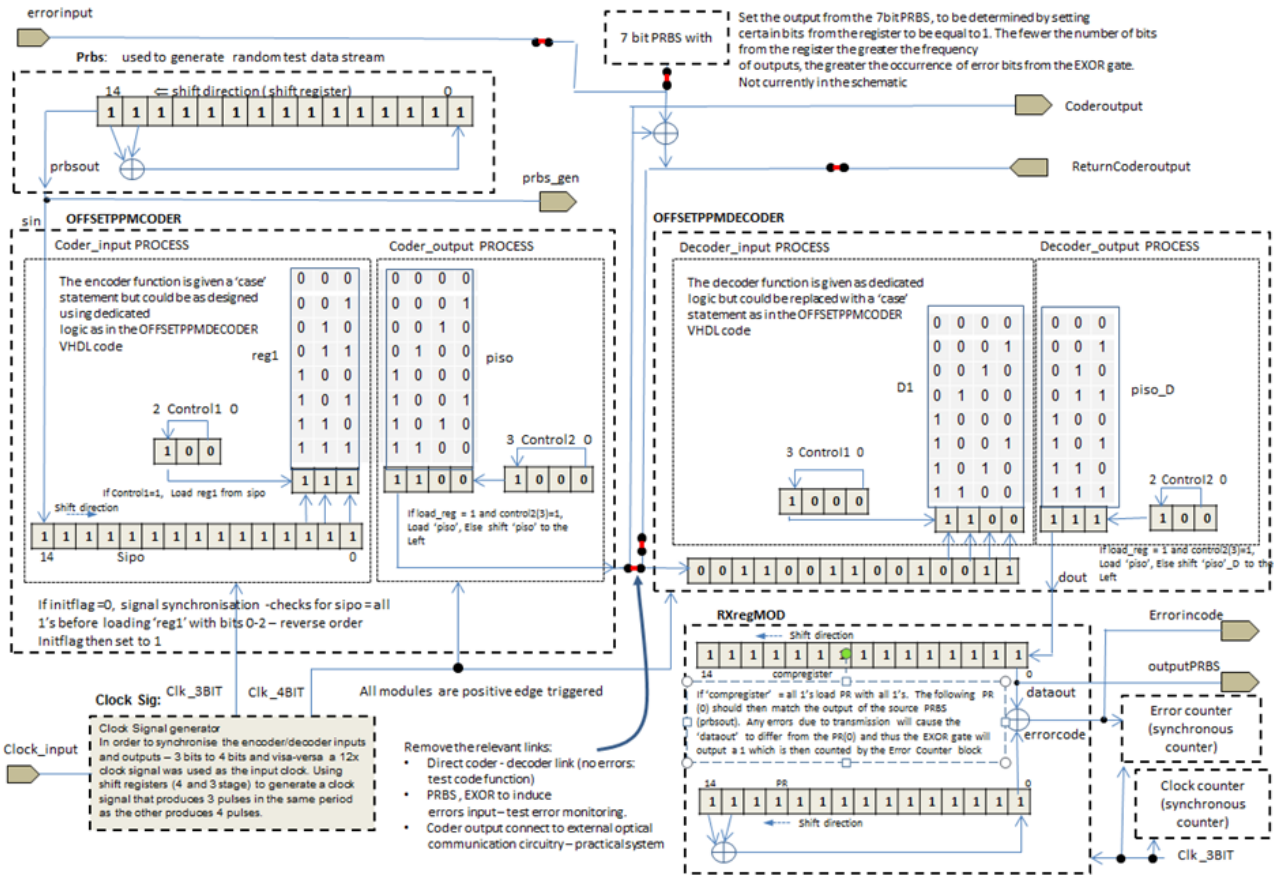

Fig. 2. Offset PPM VHDL code sequence [12]

Table 1. PCM to OPPM and DPPM Transformation

PCM (Data Word)	OPPM Code Word	DPPM Code Word
000	0 000	0000 0001
001	0 001	0000 0010
010	0 010	0000 0100
011	0 100	0000 1000
100	1 000	0001 0000
101	1 001	0010 0000
110	1 010	0100 0000
111	1 100	1000 0000

For the first time, PPM was successfully implemented on a Visible Light Communication (VLC) system using a 'warm' 30W LED, obtaining a data throughput of 11 Mbps with zero errors in transmission over a 1 m space that is free. Automatic Repeat Request (ARQ) is the name of a technology that was introduced by Wang, Cheng, Sun, and Zhang to address OPPM fault sources. They proved that OPPM has built-in error-checking capabilities and that by utilizing ARQ as a method OPPM's frame error rate performance can be improved if an error is found. OPPM Error Source, Similar to digital PPM, OPPM has three different methods of detecting failures: improper slot, wipe, and false alert. [13].

The logic gate is a typical example of a virtual instrument, which can be found in digital electronics. To carry out its operations, it makes use of a Boolean function. One logical output can be produced by the logic gate using only one logical input, while another can be produced using several logical inputs and performing a single logical operation on each of them. An important phase in the design process is the truth table for the digital circuit. This is done so that additional information may be collected at the early step of constructing a digital circuit, which entails looking at the truth table of the circuit. In other words, this is done so that more information can be obtained [14].

Table 2 displays the truth table that was generated as a result of converting the three-bit design for offset pulse position modulation (offset PPM) to pulse code modulation (PCM) (2). Truth tables reveal that a three-pin input is used to generate the digital electrical circuit in question. Figure 1 shows that the digital electrical circuit has been built with a 4-pin output. All eight states are represented by the inputs. The binary code (000) is used to represent these states in order, beginning with the first and ending with the last (111) [15].

Table 2. Truth table of Offset PPM encoder

Steps	Input/PCM (3 pins)			Output/Offset PPM (4pin)			
	A	B	C	D	E	F	G
1	0	0	0	0	0	0	0
2	0	0	1	0	0	0	1
3	0	1	0	0	0	1	0
4	0	1	1	0	1	0	0
5	1	0	0	1	0	0	0
6	1	0	1	1	0	0	1
7	1	1	0	1	0	1	0
8	1	1	1	1	1	0	0

The output of the encoder is a parallel connector with four pins. According to what is displayed up top, this analysis has resulted in the production of a total of four Boolean equations based on the data included in the truth table. These equations are enumerated in the following list, with each equation corresponding to one of the four pins:

$$D = A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC \quad (1)$$

$$E = \bar{A}BC + ABC \quad (2)$$

$$F = \bar{A}B\bar{C} + AB\bar{C} \quad (3)$$

$$G = \bar{A}\bar{B}C + A\bar{B}C \quad (4)$$

The solutions to the four equations presented earlier make it abundantly evident that to construct the coding circuit, one gate with four inputs, three three-input AND gates, and ten three-input OR gates are necessary (2-input OR gate). It is possible to simplify Boolean equations by using a tool called the Karnaugh map, which is also referred to as the K-map and may be found online. This tool is helpful for both users and academics. As a result, the Karnaugh map method was applied in this study to bring the aforementioned four equations down to a more manageable level [16].

As a consequence of this, it is very evident that to finish the building of the encoder of Offset PPM and convert its three-bit PCM input to a four-bit output, you will want three gates with two inputs per AND gate as well as two inverters. The application known as the Karnaugh map has been employed at this point to simplify things as much as is humanly practical. The Offset PPM encoder that is supposed to code a 3-input PCM needs a total of three AND gates with two inputs as well as two inverters [17]. The physical layout of the encoder of the Offset PPM circuitry has been depicted in Fig. 3, which may be seen here.

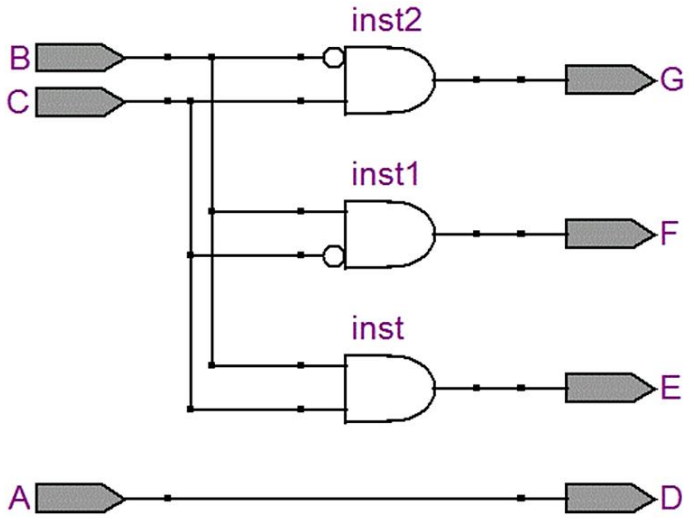

Fig. 3. Offset PPM Encoder's Electrical circuit

To practically simplify the architecture regarding PPM Decoder, the Karnaugh map was utilized [18]. The investigation revealed that there must be a total of seven AND gates with three pins, three OR gates with two pins, and one OR gate with three pins. Fig. 4 presents the schematic layout of the Offset PPM Decoder's circuitry [19].

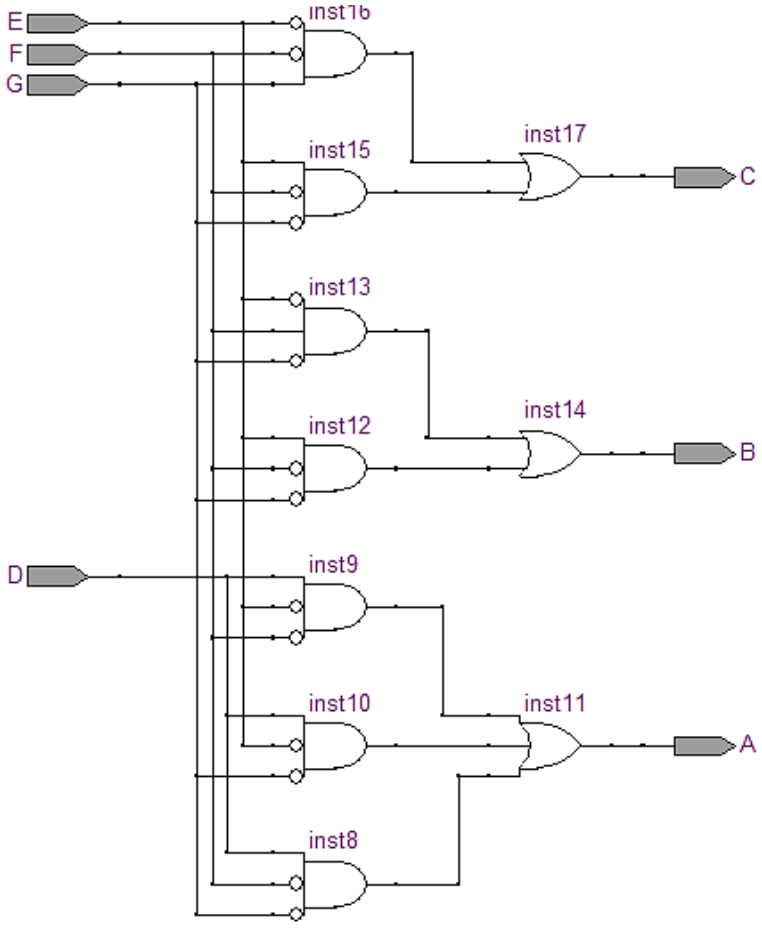

Fig. 4. Offset PPM Decoder schematic [20]

2. Proposal System

The architecture of the OPPM system, which makes use of RS coding, is shown in Fig. 5. The pseudo-random binary sequence (PRBS) block, which is located at the transmitter, which is generating a unique PCM message with k equal to 23 symbols. Whenever the PCM message is encoded with the (31,23) RS coder, redundancy symbols with a total of n-k=8 symbols are added to the message. For the output of the parallel

RS coder to be suitable for use as the input for the OPPM coder, it must first be converted to serial format by the bridge coder. Upon arrival at the receiver, the OPPM decoder interprets the message and converts it into PCM format using the OPPM pulses (Truth Table achieve). After that, the bridge decoder is utilized to do the serial-to-parallel PCM conversion. The final stage is the employment of a (31,23) RS decoder, which is utilized to retrieve the initial message.

We presumed that the system described below for the correction and detection of mistakes that are associated with offset pulse position modulation (OPPM) would work and be programmed in VHDL. Erasure of the erroneous VHDL code would take place when the location of the incorrect symbol was known. A decoder has the capability of erasing or correcting up to t mistakes simultaneously. Information can frequently be forwarded to the receiver. This occurs when the receiver "Decode OPPM" receives symbols that possibly include some errors and then sends the stream of data on to the next block for matching and comparing the source data with the received data to determine in which location the bit error is present. The structure of an implemented Reed-Solomon algorithm with modulation offset PPM is shown in Fig. 5.

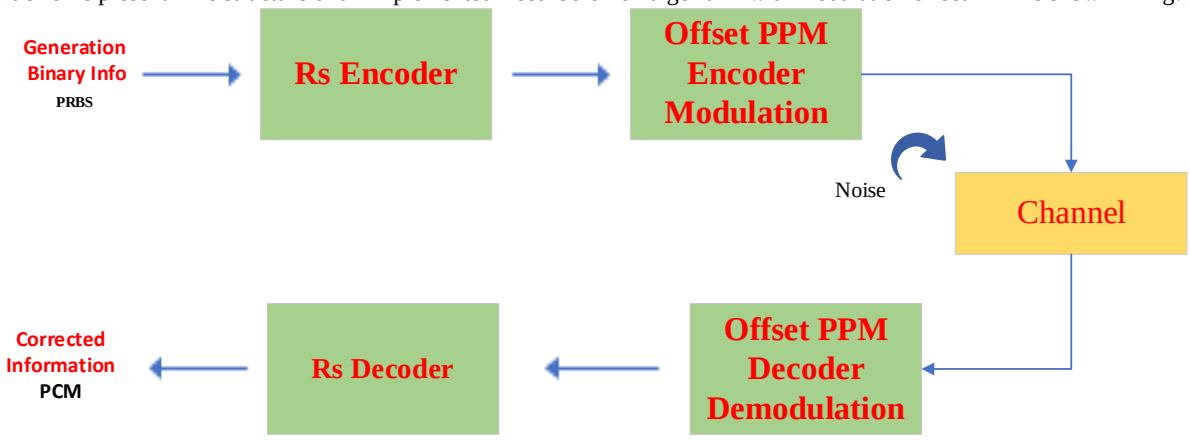

Fig. 5. illustrates the structure of implemented Reed-Solomon with modulation offset PPM

3. Results and Discussion

Reed Solomon's error correcting system, which is precisely represented in the RS encoder out and has a maximum frequency of 50 MHz, has received an input signal, which is shown in Fig. 6 as the RS coder serial waveform in both multi and single modes. codeword mode. After converting the output of the parallel RS coder using the bridge code, the serial data was gathered after conversion. The findings of the comprehensive test of the Offset PPM system simulation are depicted in Fig. 7. The signal that is transmitted from the Offset PPM Decoder is the same as the RS ENCODER OUTPUT signal, except for the fact that it is delayed. Synchronization between the parallel 3-bit word and the 5-bit word was able to be accomplished because of the signals that were generated by the clocks. The figure below shows both the parallel output of the RS encoder and the parallel output of the RS decoder, Fig. 8.

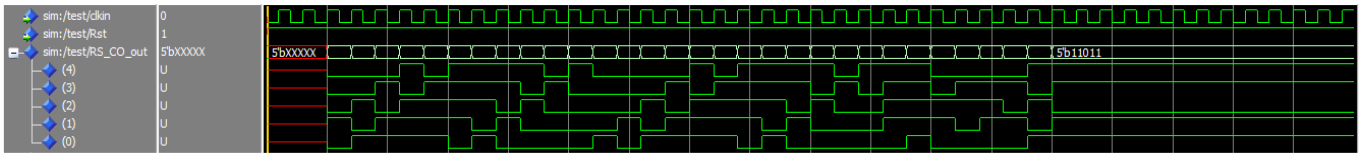

Fig. 6. Input signal and output Reed Solomon Encoder Simulation

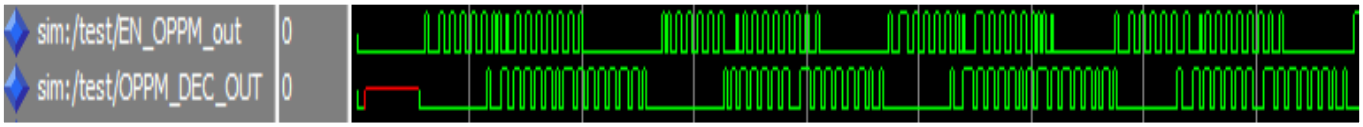

Fig. 7. Output of Encoding and Decoding of OPPM use ModelSim

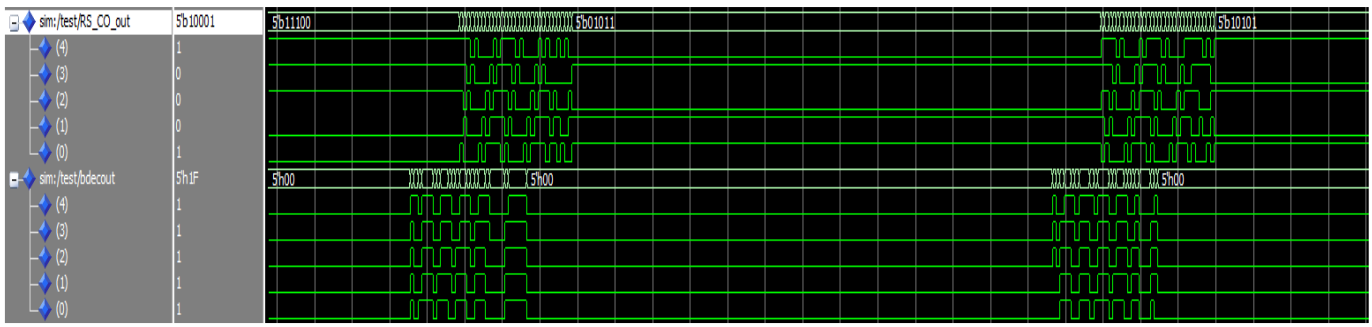

Fig. 8. Coder and decoder Reed Solomon Simulation

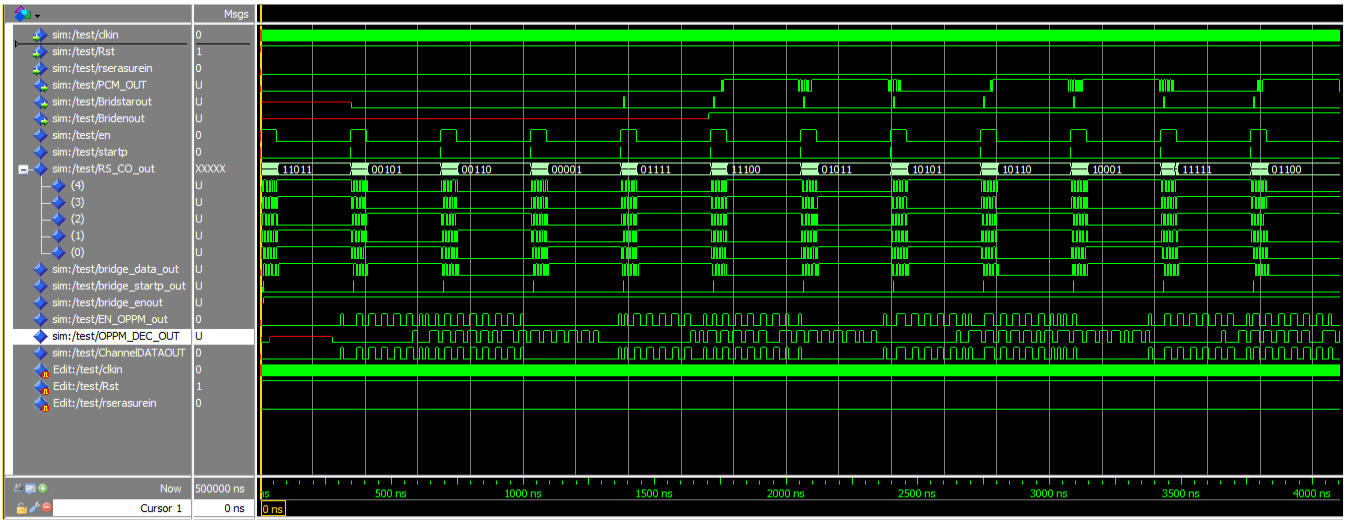

Fig. 9. System coder I/O waveform

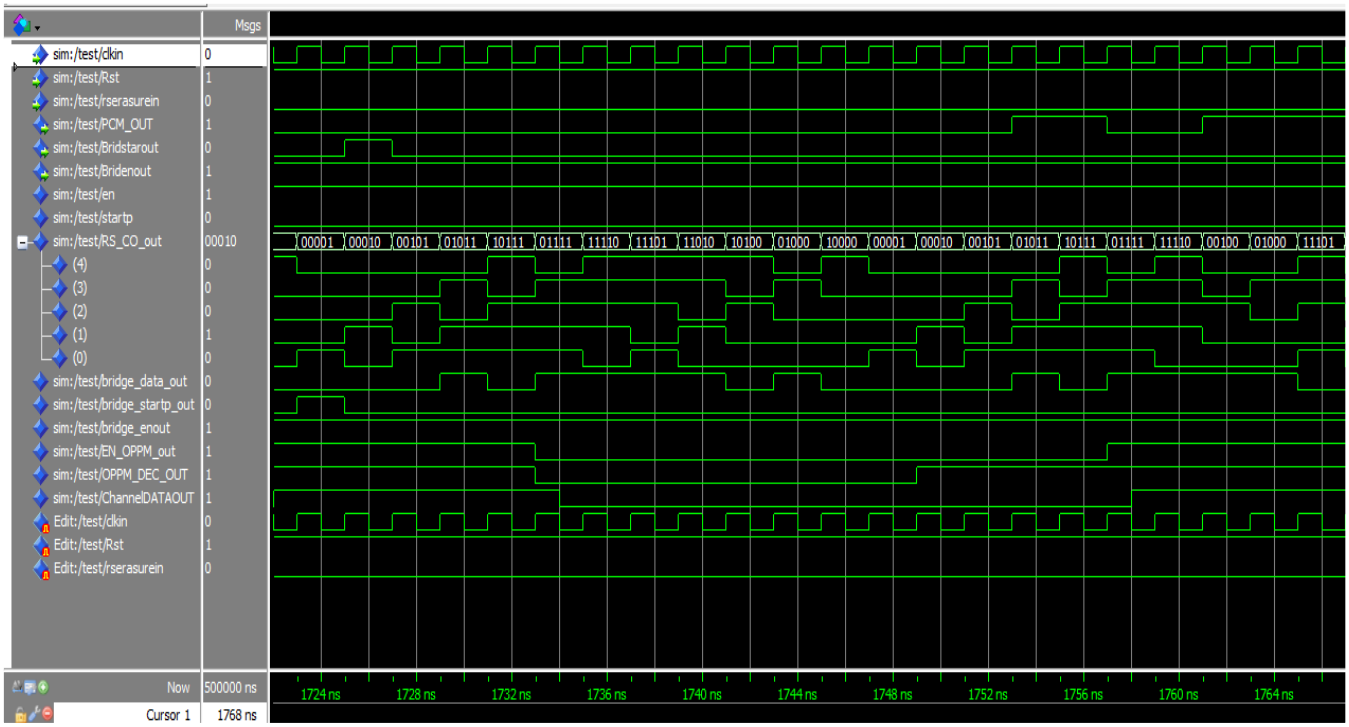

Fig. 10. System coder I/O waveform one codeword zoom

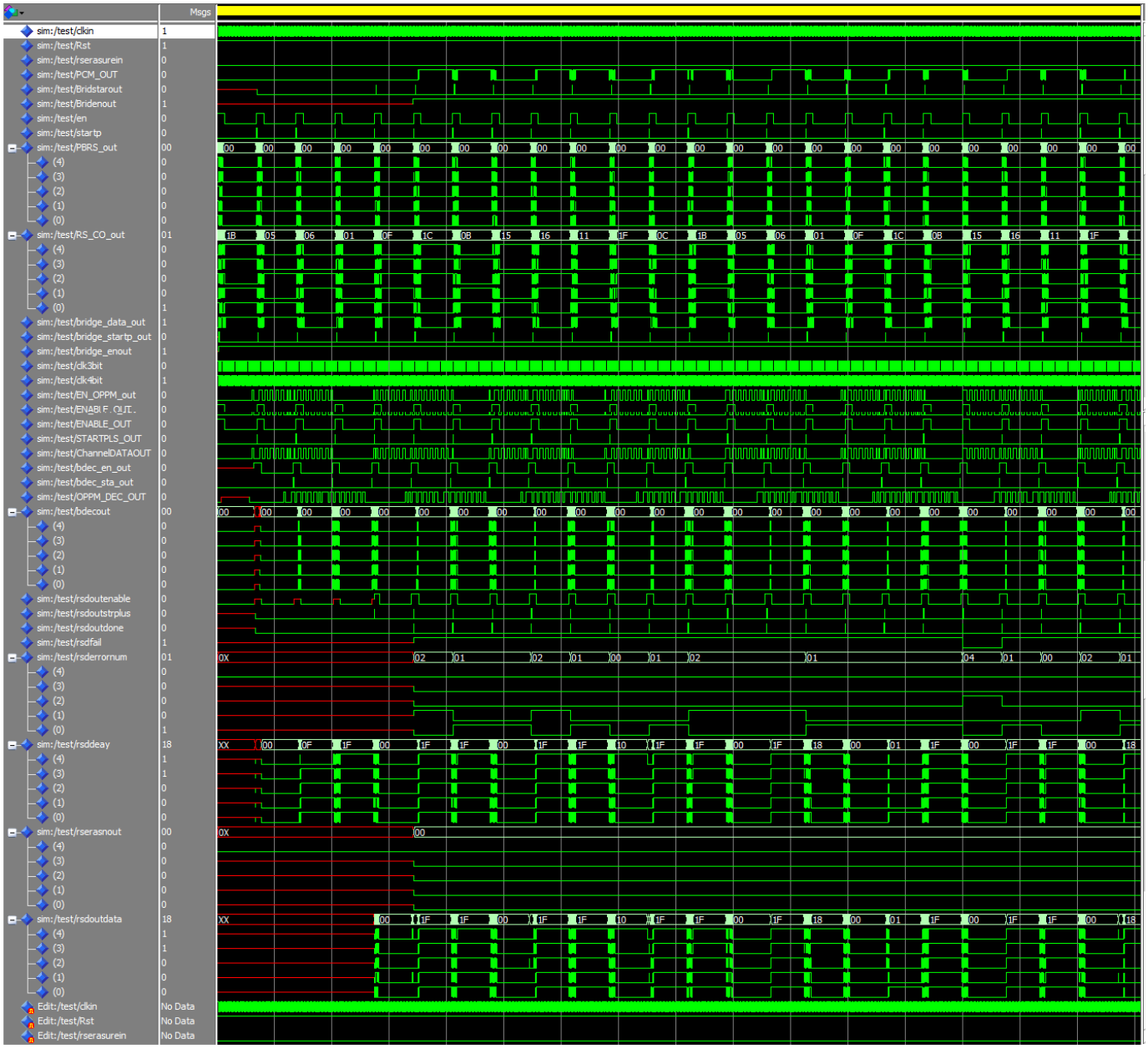

Fig. 11. All System block encoder and decoder simulation

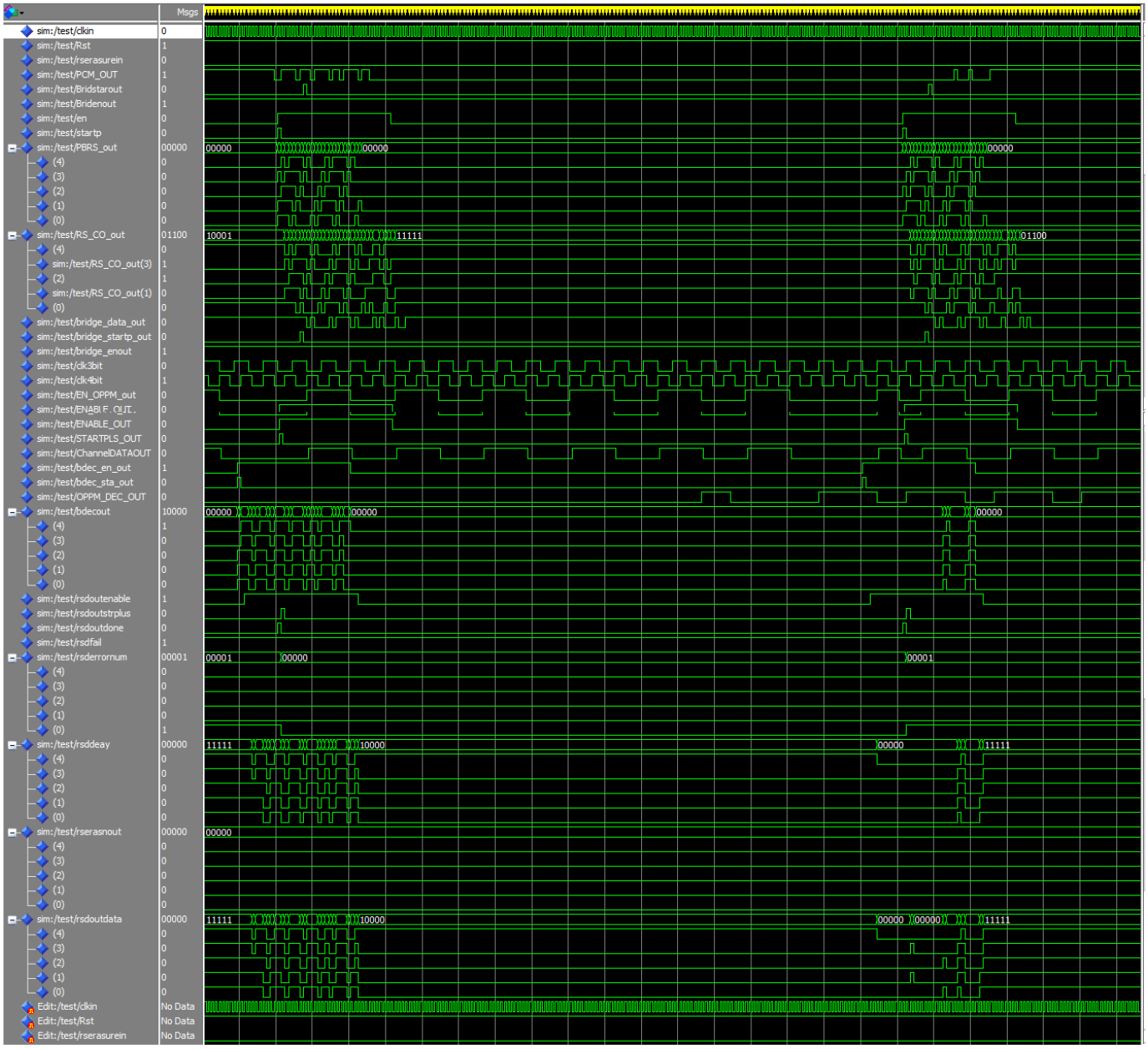

Fig. 12. All pin's input and output simulation Zoom

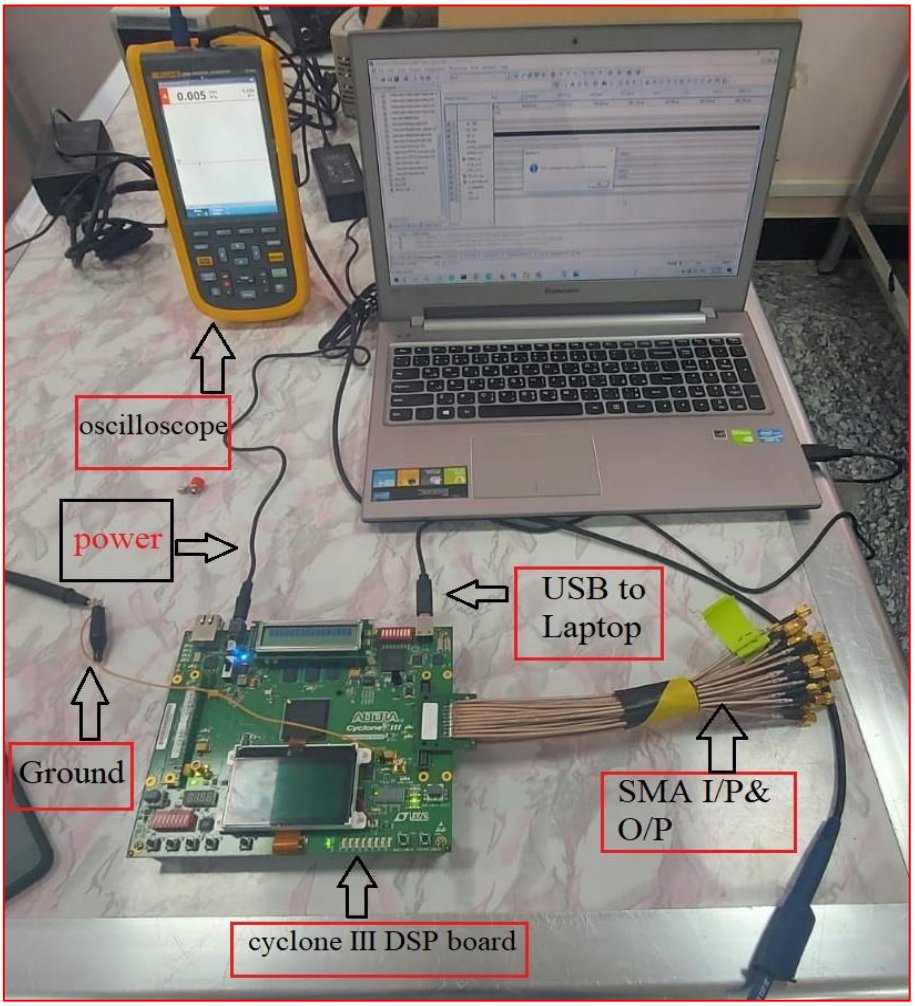

Fig. 13. Facility for testing a design on a cyclone III board in a lab

4. Conclusions

Reed-Solomon codes are a type of error-correcting code that are block-based and have a wide variety of applications in digital communications as well as storage. The implementation of these programs using FPGA technology offers several benefits, including efficient reconfigurability and universal chip implementation, amongst others. Writing hardware description programs (using a language like VHDL) for each component in the system and the main program to govern the influence of signals in the system is the first step that is included regarding the design process when utilizing FPGA Technology. This step is part of the design method. After that, a top-level schematic design is needed to describe the pins that are necessary for the actual hardware interface. A programming file is eventually downloaded to the FPGA board once the compilation has been completed successfully, timing analysis has been obtained, and synthesis reports have been generated. Within the scope of this study, the system source code modulation via offset PPM has been presented. The VHDL language has been used to describe every component of the system. The system has been designed with the parameters that produce the best results from the Reed Solomon code. The results of the simulation demonstrated that all of the components of the system are functioning appropriately and agreed with the theory underlying the system. In this particular piece of study, the signal of Offset PPM was developed by Reed Solomon and is being utilized for the very first time as a novel mechanism.

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